IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

FLYNN et al — Atty. Ref.: 550-466

Serial No. 10/691,501 — Group: 2189

Filed: October 23, 2003 — Examiner: Dinh, Ngoc V.

For: HARDWARE DRIVEN STATE SAVE/RESTORE IN A DATA PROCESSING SYSTEM

Before the Board of Patent Appeals and Interferences

BRIEF FOR APPELLANT

On Appeal From Final Rejection
From Group Art Unit 2189

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October 15, 2007

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF

I. REAL PARTY IN INTEREST

The real party in interest is the assignee, ARM Limited, a United Kingdom corporation.

II. RELATED APPEALS AND INTERFERENCES

There are no other appeals related to this subject application. There are no interferences related to this subject application.

III. STATUS OF CLAIMS

Claims 1-24 are pending, rejected, and on appeal.

IV. STATUS OF AMENDMENTS

No amendments after final were filed. A pre-appeal was filed on June 18, 2007.

V. SUMMARY OF THE CLAIMED SUBJECT MATTER

A data processing system should be able to save and restore its system state. One situation where this is helpful is in a power saving or power-down mode. For example, if the system detects its been idle for a predetermined amount of time or that a power down key was pressed, the system can switch to a power-down mode. But when the power-down mode is exited, the system should return to its previous state unaltered so that processing operations can continue smoothly and efficiently. Otherwise, if the information/state is lost upon exiting the power-down mode, a full system reboot and initialization upon restart must be performed.

One approach to power-saving power-down uses a power-down software routine executed when entry to the power-down mode is required. The routine saves to some non-volatile storage data thereby capturing the state of the system. A complementary piece of software can be run when the system resumes operation to restore this state information from the non-volatile storage so that processing can be recommenced at the same point and with the same system state. But significant disadvantages with this approach include slow software routine execution, both to store the system state and then to later restore the system state.

Furthermore, there may be some system state information which is not accessible to the software responsible for saving the system state, such as for example cache memory contents, tightly-coupled memory content, and other, relatively low level hardware state information. In such circumstances, when processing is resumed, it recommences in a way that only approximates the state of the system when power-down occurred, such as for example there being a requirement to refill all of the cache memories, which may be a relatively slow and power consuming operation. Furthermore, on restarting the system some state, such as a page table mapping, which is required for a simple restart, is not available.

The inventors found a better way to save off data values representing the system state using the existing system bus and memory within a data processing system under the control of state saving controller hardware. Surprisingly, by reusing the already-provided system bus and memory, the state saving controller can be simple and yet rapidly and efficiently save and later restore the system state with an advantageous degree of completeness.

The following is a mapping of independent claim 1 onto an example, non-limiting embodiment in the specification.[1]

[1] This mapping in no way limits the claim scope and is not intended to be used in construing the meaning of claim terms. Indeed, another non-limiting example embodiment is described in conjunction with Figure 5.

Apparatus for processing data, comprising:	Figure 2.
a circuit used in processing data, said circuit having one or more nodes for storing one or more data values that together define a state of said circuit;	Processor core 2 stores one or more data values in one or more nodes like registers, program counters, etc. coupled to scan chains 12. See Figure 3 and page 8, lines 4-6 and 12-14.
a memory for storing data;	Memory 14 in Figure 3. See page 8, lines 4-6.
a multi-bit wide system bus, coupled to said circuit and said memory, for transferring multi-bit data words between said circuit and said memory in response to memory transfer requests issued upon said system bus during normal processing operation of said circuit and said memory; and	A multi-bit wide system bus 6 , 8, and 10 couples core 2 and memory 14 and transfers multi-bit data words between the circuit and memory in response to memory transfer requests issued upon the bus 6 during normal processing operation. Page 8, lines 15-17.
a state saving controller, coupled to said circuit and said system bus, configured in response to a state saving trigger to read said data values defining a state of said circuit from said one or more nodes and to generate a sequence of memory write requests on said system bus that write one or more state saving multi-bit data words representing said data values into said	State saving controller 16 responds to a state saving trigger to read said data values defining a state of said circuit from one or more nodes coupled to a scan chain 12. The controller 16 then clocks the scan chains 12 to form the state saving data words and generate the address control signal on the bus to cause a

memory such that said state of said circuit is restorable using said one or more state saving multi-bit data words.	data transfer from the core 2 to memory 14. A restore operation is described at page 8, lines 27-32.

Because independent method claim 13 is a method analog of apparatus claim 1, the mapping provided for claim 1 also applies to independent claim 13.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The rejection on appeal includes the rejection of claims 1-7, 9,11, 12, 13-19, 21, 23, and 24 under 35 U.S.C. §102 as being anticipated by Godfrey (USP 6,550,031).

VII. ARGUMENT

A. The Legal Requirements For Anticipation

To establish that a claim is anticipated, the Examiner must point out where each and every limitation in the claim is found in a single prior art reference. *Scripps Clinic & Research Found. v. Genentec, Inc.*, 927 F.2d 1565 (Fed. Cir. 1991). Every limitation contained in the claims must be present in the reference, and if even one limitation is missing from the reference, then it does not anticipate the claim. *Kloster Speedsteel AB v. Crucible, Inc.*, 793 F.2d 1565 (Fed. Cir. 1986). Godfrey fails to satisfy this rigorous standard.

B. Godfrey's System Bus 100 Is Not Coupled To the Memory 200

The independent claims require "a multi-bit wide system bus, coupled to said circuit and said memory, for transferring multi-bit data words between said circuit and said memory in response to memory transfer requests issued upon said system bus during normal processing operation of said circuit and said memory." Quoted from claim 1. The Examiner maps the claimed memory to the external memory 200 shown in Figure 2 of Godfrey and the claimed multi-bit wide system bus to the internal bus 100. Figure 2 reproduced below clearly shows that the internal bus 100 (the thickest black line) is not coupled or connected to the external memory 200. Only the SCAN_PATH[2] (the medium thickness black line) is connected to the external memory 200 and to the device state registers 104a, 108a, 112a, etc. The SCAN_PATH is not shown or described as connected to the internal bus 100. The internal bus 100 is only shown coupling the peripheral devices to each other and the execution unit 124.

[2] The SCAN_PATH cannot be the claimed system bus that transfers multi-bit wide data words, meaning that multiple bits are transferred in parallel, because the one wire scan path transfers data serially. See e.g., 4:48-65.

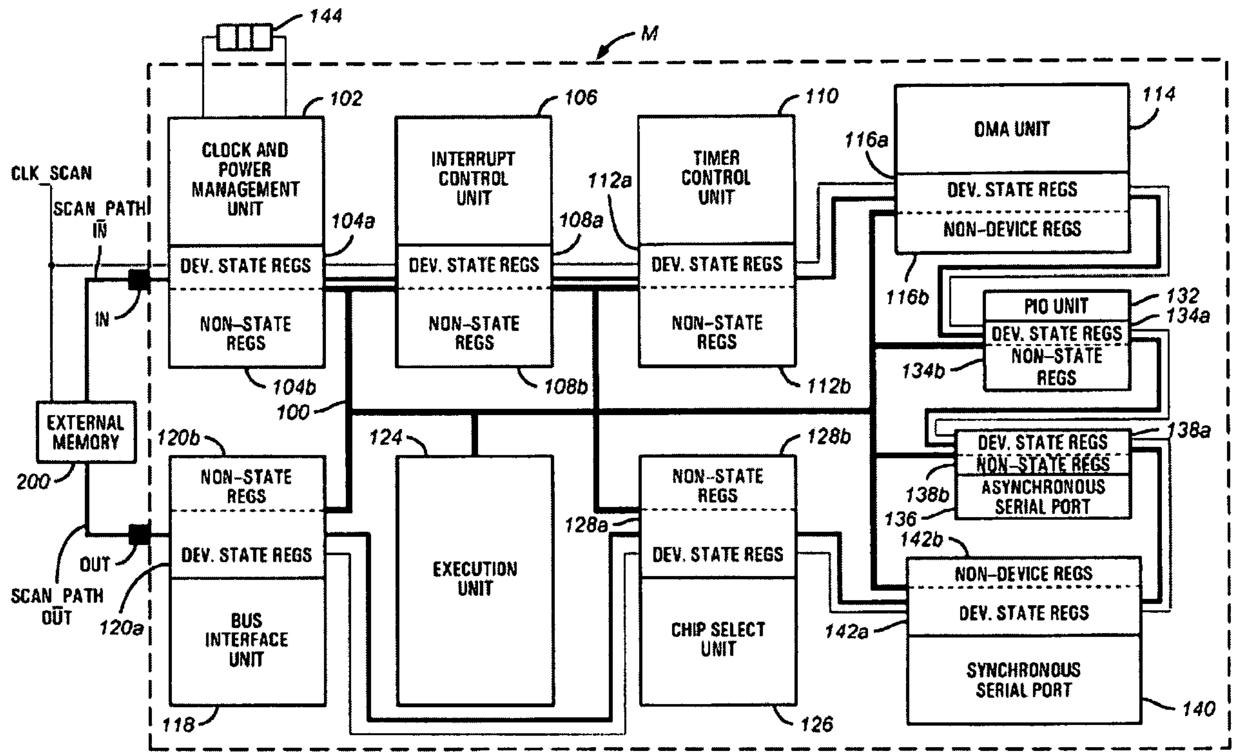

FIG. 2

The SCAN_PATH is clearly a separate path from the internal bus 100. A <u>single</u> configuration scan data out pin OUT is coupled to the external memory 4:65-67, and the configuration scan data from each peripheral is "sequentially shifted out of each configuration register into external memory 200 via SCAN_PATH." 4:67-5:2. Similarly, "the external memory 200 is coupled to the input pin IN, so that configuration scan data from external memory 200 can be synchronously shifted into each peripheral configuration register via SCAN_PATH." Col. 5, lines 3-6. Nor is there disclosure of the internal bus 100 being coupled to the SCAN_PATH.

C. Godfrey's System Bus 100 Does Not Transfer Multi-Bit Data Words Between The Circuit And The Memory 200

During normal operation, the internal bus 100 of Godfrey does not transfer multi-bit data words between the claimed circuit (the elements within the dotted line of Figure 2 labeled as the microcontroller M) and the external memory 200 in response to memory transfer requests issued upon the internal bus 100. The internal bus 100 communicates with the various peripherals and the execution unit 124 shown as coupled to bus 100 in Figure 2, i.e., the elements within the dotted line. But this circuit M defined by the dotted line box does not include the external memory 200.

The Examiner makes reference to 3:65-4:5. Here Godfrey states:

> The microcontroller M preferably includes an internal bus 100 coupling a variety of functional units and registers (herein referred to as peripheral devices except the execution unit), used to control and monitor those units. These peripheral devices include a clock and power management unit 102 with corresponding clock/power registers 104.

Nothing in this text teaches that Godfrey's internal system bus 100 transfers multi-bit data words between the circuit M defined by the dotted line box and the external memory 200 outside of the dotted line box.

The external memory 200 is only connected to the serial SCAN_PATH. Godfrey does not teach using the SCAN_PATH during normal processing

operations. As noted above, the SCAN_PATH in Godfrey is a single bit-wide data path and does not transfer multi-bit data words.

The Examiner references 5:22-25 and 8:12, 13, 34, and 35. At 5:22-25, Godfrey describes that a function of a UART peripheral to convert data between serial and parallel form. A UART is not relevant to the claims. The text at 8:12, 13, 34, and 35 relates to parallel transfer between state register stages and registers. But the question is what is the bus width of the scan data communicated between the microcontroller M and the external memory 200. The answer is a single bit (serial) and not multi-bit.

D. Godfrey Does Not Transfer The State Information To/From Memory Using The Multi-Bit Wide System Bus.

The independent claims also require:

> a state saving controller, coupled to said circuit and said system bus, configured in response to a state saving trigger to read said data values defining a state of said circuit from said one or more nodes and to generate a sequence of memory write requests on said system bus that write one or more state saving multi-bit data words representing said data values into said memory such that said state of said circuit is restorable using said one or more state saving multi-bit data words.

Quoted from claim 1. The Examiner maps the state saving controller onto the microcontroller M which applies a trigger to the state registers. The Examiner refers to 8:54-60 as disclosing the use of the system bus 100 for writing one or more state-saving, multi-bit data words into the external memory 200. But it is the

serial SCAN_PATH coupled to the external memory 200 that takes signal values from the configuration registers and saves them in the external memory 200 or loads them back from the external memory 200. These writes to and reads from the external memory 200 do not take place using the multi-bit wide system bus 100.

The technology defined by the independent claims reuses the system bus and the memory to provide state saving functionality with speed and efficiency. Godfrey's single bit wide serial scan chain is significantly slower than a multi-bit wide system bus in performing such state saving and restore operations. Furthermore, the serial scan chain of Godfrey is a separate structure provided, at least partially, for this purpose and is not used during normal processing operations. Consequently, Godfrey's serial scan chain is an additional circuit overhead.

VIII. CONCLUSION

The anticipation rejection is in error because Godfrey lacks features from the independent claims. The absence of even one claim feature from a prior art reference defeats an anticipation rejection. The Board should reverse the rejection and order the application allowed.

Respectfully submitted,

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JRL/maa
Appendix A - Claims on Appeal

IX. CLAIMS APPENDIX

1. (Previously presented) Apparatus for processing data, comprising:

a circuit used in processing data, said circuit having one or more nodes for storing one or more data values that together define a state of said circuit;

a memory for storing data;

a multi-bit wide system bus, coupled to said circuit and said memory, for transferring multi-bit data words between said circuit and said memory in response to memory transfer requests issued upon said system bus during normal processing operation of said circuit and said memory; and

a state saving controller, coupled to said circuit and said system bus, configured in response to a state saving trigger to read said data values defining a state of said circuit from said one or more nodes and to generate a sequence of memory write requests on said system bus that write one or more state saving multi-bit data words representing said data values into said memory such that said state of said circuit is restorable using said one or more state saving multi-bit data words.

2. (Original) Apparatus as claimed in claim 1, wherein said circuit is a processor core.

3. (Original) Apparatus as claimed in claim 1, wherein said one or more nodes are each coupled to a respective scan chain cell within said circuit, said state saving controller being operable in response to said state saving trigger to store said data values within respective scan chain cells and to serially read said data values from said scan chain cells to form said one or more state saving multi-bit data words.

4. (Original) Apparatus as claimed in claim 3, comprising a plurality of scan chains each containing a plurality of scan chain cells, said plurality of scan chains operating in parallel to provide respective bits that together form a state saving multi-bit data word as said plurality of scan chains of serially read.

5. (Original) Apparatus as claimed in claim 3, wherein said scan chain cells are also operable to perform test functions upon said circuit.

6. (Original) Apparatus as claimed in claim 1, wherein said circuit is a further memory and said data values are bits of data words stored in said further memory.

7. (Original) Apparatus as claimed in claim 6, wherein said further memory is coupled to a built-in self-test controller operable to perform self-test operations upon said further memory and said state saving controller uses said built-in self-test controller to read data values from said further memory to form said state saving multi-bit data words.

8. (Original) Apparatus as claimed in claim 1, wherein said memory transfers are burst mode memory transfers.

9. (Original) Apparatus as claimed in claim 1, wherein said state saving controller is operable in response to a state restoring trigger to generate a sequence of memory read requests on said system bus that read said one or more multi-bit state saving data words from said memory via said system bus and write said data values represented by said multi-bit state saving data words to said one or more nodes to thereby restore said state of said circuit.

10. (Original) Apparatus as claimed in claim 1, wherein said multi-bit state saving data words are stored in a user specified region of said memory.

11. (Original) Apparatus as claimed in claim 1, wherein said state saving trigger comprises execution of a state saving program instruction.

12. (Original) Apparatus as claimed in claim 1, wherein said state saving trigger comprises initiation of a diagnostic test upon said circuit.

13. (Original) A method of saving state within an apparatus for data processing having:

a circuit used in processing data, said circuit having one or more nodes operable to store one or more data values that together define a state of said circuit;

a memory operable to store data; and

a system bus coupled to said circuit and said memory and operable to transfer multi-bit data words between said circuit and said memory in response to memory transfer requests issued upon said system bus during normal processing operation of said circuit and said memory; said method comprising:

in response to a state saving trigger, using a state saving controller coupled to said circuit and said system bus to read said data values defining a state of said circuit from said one or more nodes and to generate a sequence of memory write requests on said system bus that write one or more state saving multi-bit data words representing said data values into said memory such that said state of said circuit is restorable using said one or more state saving multi-bit data words.

14. (Original) A method as claimed in claim 13, wherein said circuit is a processor core.

15. (Original) A method as claimed in claim 13, wherein said one or more nodes are each coupled to a respective scan chain cell within said circuit, said state saving

controller being operable in response to said state saving trigger to store said data values within respective scan chain cells and to serially read said data values from said scan chain cells to form said one or more state saving multi-bit data words.

16. (Original) A method as claimed in claim 15, comprising a plurality of scan chains each containing a plurality of scan chain cells, said plurality of scan chains operating in parallel to provide respective bits that together form a state saving multi-bit data word as said plurality of scan chains of serially read.

17. (Original) A method as claimed in claim 15, wherein said scan chain cells are also operable to perform test functions upon said circuit.

18. (Original) A method as claimed in claim 13, wherein said circuit is a further memory and said data values are bits of data words stored in said further memory.

19. (Original) A method as claimed in claim 18, wherein said further memory is coupled to a built-in self-test controller operable to perform self-test operations upon said further memory and said state saving controller uses said built-in self-test controller to read data values from said further memory to form said state saving multi-bit data words.

20. (Original) A method as claimed in claim 13, wherein said memory transfers are burst mode memory transfers.

21. (Original) A method as claimed in claim 13, wherein said state saving controller is operable in response to a state restoring trigger to generate a sequence of memory read requests on said system bus that read said one or more multi-bit state saving data words from said memory via said system bus and write said data values represented by said multi-bit state saving data words to said one or more nodes to thereby restore said state of said circuit.

22. (Original) A method as claimed in claim 13, wherein said multi-bit state saving data words are stored in a user specified region of said memory.

23. (Original) A method as claimed in claim 13, wherein said state saving trigger comprises execution of a state saving program instruction.

24. (Original) A method as claimed in claim 13, wherein said state saving trigger comprises initiation of a diagnostic test upon said circuit.

X. EVIDENCE APPENDIX

There is no evidence appendix.

XI. RELATED PROCEEDINGS APPENDIX

There is no related proceedings appendix.